

## Introduction

### WCET Analysis

- ▶ Timing-critical applications
  - ▶ Strict deadlines on the response times
- ▶ WCET bound of a program
  - ▶ Upper bound on the execution times
  - ▶ Depends on behavior at microarch. level
  - ▶ Obtained by **WCET analysis**
- ▶ Modern processors are complex
  - ▶ Designed for average-case performance
  - ▶ Too many behaviors at microarch. level
  - ▶ Exhaustive simulation not possible
- ▶ Need for **approximation**
  - ▶ Hide some microarchitectural details

### Multi-Core Processors

- ▶ Resources shared between the cores
  - ▶ Data buses
  - ▶ Caches
- ▶ Advantages
  - ▶ Reduced weight
  - ▶ Reduced energy consumption
  - ▶ Reduced production costs
- ▶ Shared resource **interference**
  - ▶ Performance can drop
- ▶ Challenge for WCET analysis
  - ▶ Consider all access interleavings
- ▶ Need for **approximation**

### Existing Approaches

- ▶ Limited to particular...
  - ▶ ...classes of processors
  - ▶ ...ways of approximation
- ▶ Formalisms and algorithms differ
- ▶ Yet, they follow a **common methodology**
  - ▶ Coarse approximation as baseline
  - ▶ Exclude some spurious behavior

### Our Contribution

- ▶ A **meta approach**
  - ▶ Formalizes common methodology

## Meta Approach

- ▶ For simplicity
  - ▶ One program per core
  - ▶ Each program is run at most once
- ▶ Concrete execution behavior of given system

$$Traces \subseteq Universe$$

- ▶ WCET of program on core  $C$

$$WCET_C = \max_{t \in Traces} et_C(t)$$

- ▶ Approximation by abstract traces

- ▶ Abstract model  $(\widehat{Traces}, \gamma_{trace})$

- ▶ Overapproximates concrete behavior

$$\bigcup_{\hat{t} \in \widehat{Traces}} \gamma_{trace}(\hat{t}) \supseteq Traces$$

- ▶ Provides WCET bound

$$\max_{\hat{t} \in \widehat{Traces}} UB et_C(\hat{t}) \geq WCET_C$$

- ▶ Infeasible abstract traces

$$\widehat{Infeas} = \{\hat{t} \mid \hat{t} \in \widehat{Traces} \wedge \gamma_{trace}(\hat{t}) \cap Traces = \emptyset\}$$

- ▶ Only describe spurious behavior
- ▶ May dominate WCET bound calculation

- ▶ System properties

$$Prop = \{P_1, \dots, P_{\#Prop}\}$$

- ▶ Hold for each system behavior

$$\forall t \in Traces : \forall P_i \in Prop : P_i(t)$$

- ▶ Lifting properties to abstract traces

- ▶ Soundness criterion for lifted version  $\widehat{P}_i$  of  $P_i$

$$[\exists t \in \gamma_{trace}(\hat{t}) : P_i(t)] \Rightarrow \widehat{P}_i(\hat{t})$$

- ▶ Detecting infeasible abstract trace  $\hat{t}$

$$[\exists P_i \in Prop : \neg \widehat{P}_i(\hat{t})] \Rightarrow \hat{t} \in \widehat{Infeas}$$

- ▶ Remove some infeasible abstract traces

$$\widehat{LessTraces} = \{\hat{t} \mid \hat{t} \in \widehat{Traces} \wedge \forall P_i \in Prop : \widehat{P}_i(\hat{t})\}$$

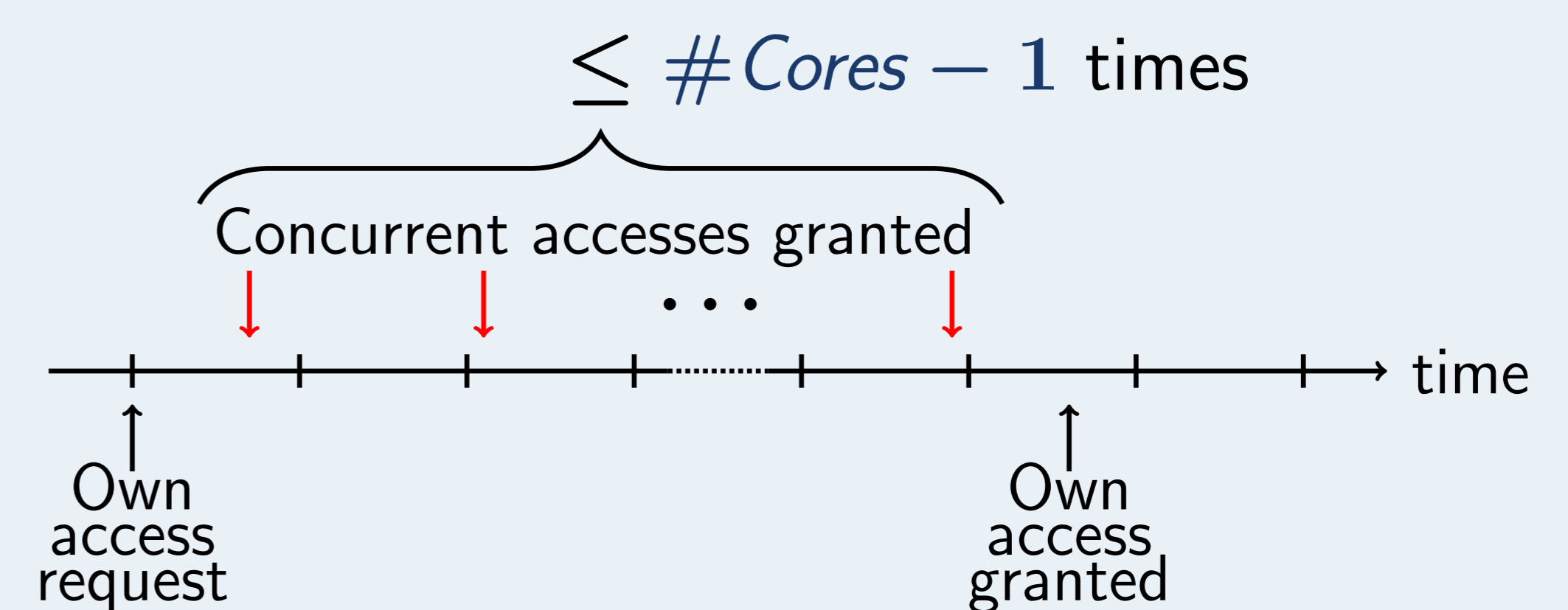
- ▶ Potentially **improved** WCET bound

$$\max_{\hat{t} \in \widehat{LessTraces}} UB et_C(\hat{t}) \geq \max_{\hat{t} \in \widehat{Traces}} UB et_C(\hat{t}) \geq WCET_C$$

## Property Lifting Example

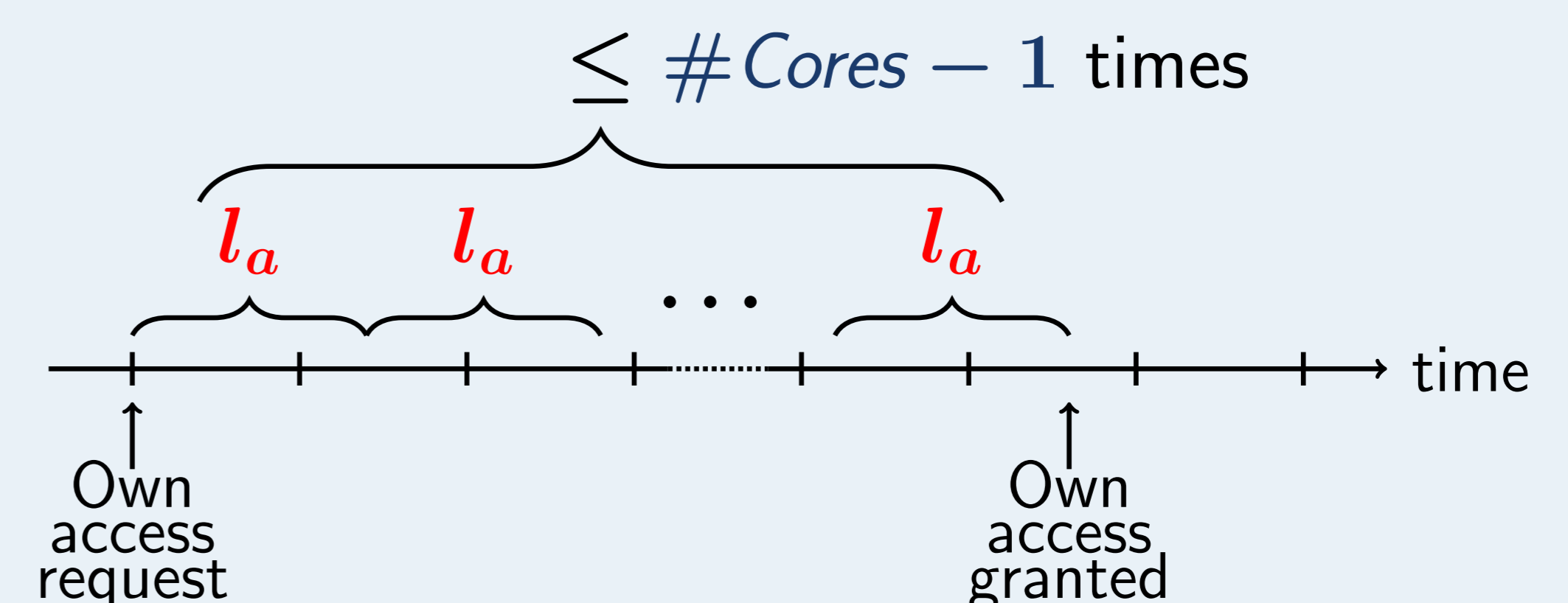
- ▶ Round-robin bus arbitration

- ▶ Before a requested bus access is granted, at most one bus access per concurrent core is granted.



- ▶ Blocked cycles for a single bus access

- ▶ No access takes longer than  $l_a$  cycles



- ▶ A round-robin property

- ▶ Shall hold for all  $t \in Traces$

$$P_{rr}(t) \Leftrightarrow [\#blockedCycles_C(t) \leq \#accesses_C(t) \cdot (\#Cores - 1) \cdot l_a]$$

- ▶ Lifting  $P_{rr}$  to abstract traces

$$\exists t \in \gamma_{trace}(\hat{t}) : P_{rr}(t)$$

$$\Leftrightarrow \exists t \in \gamma_{trace}(\hat{t}) :$$

$$\#blockedCycles_C(t)$$

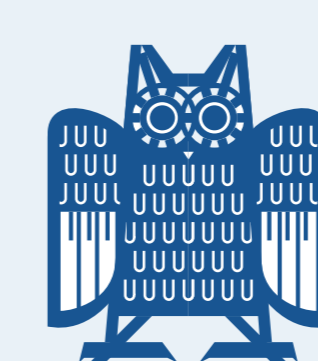
$$\leq \#accesses_C(t) \cdot (\#Cores - 1) \cdot l_a$$

$$\Rightarrow {}^{LB} \#blockedCycles_C(\hat{t})$$

$$\leq {}^{UB} \#accesses_C(\hat{t}) \cdot (\#Cores - 1) \cdot l_a$$

$$\Leftrightarrow \widehat{P}_{rr}(\hat{t})$$

## Acknowledgement



AVACS

<http://www.uni-saarland.de>

<http://www.avacs.org>